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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10 056,610	01 24 2002	Joseph M. Brand	MIO 0051 V2	1537

7590

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EXAMINER

CHAMBLISS, ALONZO

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 05 12 2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,610	BRAND, JOSEPH M.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) 1-29, 31, 35-39 and 46-49 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 30, 32-34, 40-45 and 50-52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The preliminary amendment A filed on 1/24/02 has been fully considered and made of record in Paper No. 3.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 1/24/02 in Paper No. 2 was filed before the mailing date of the non-final rejection on 5/8/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claim 30 recites the limitation " said semiconductor die " in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2827

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 30, insofar as definite, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hegel (U.S. 5,255,157).

With respect to Claim 30, Hegel teaches providing a semiconductor chip 13 and a laminate 10 defining first and second major faces, wherein the laminate 10 includes an electrically conductive layer, and an underlying substrate (i.e. the multi-layer structure) supporting the electrically conductive layer (see col. 2 lines 59-65; Fig. 4). At least one void 21 is in the laminate so as to extend from one of the major faces through the electrically conductive layer at least as far as the underlying substrate. Encapsulating the semiconductor chip 13 and the laminate 10 with an encapsulant 16 such that the encapsulant 16 extends into the void 21 to contact the underlying substrate 10 (see col. 4 lines 1-26; Fig. 4).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 32-44, 50, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hegel (U.S. 5,255,157) as applied to claim 33 above, and further in view of Juskey et al. (U.S. 5,336,931).

With respect to Claims 32 and 40, Hegel discloses a substrate 10 with a plurality of individual layers (i.e. first, second, third, and fourth laminate layers), wherein all of the layers have a void (i.e. cavity) that is over the void of the other plurality of layers. The plurality of individual layers is over one another. A conductive layer is over the fourth laminate, so as to define a void portion over the void 21 portion of the fourth laminate layer (see col. 2 lines 59-68; Fig. 4). Hegel fails to disclose forming a solder resist layer over the conductive layer, so as to define a void portion over the void portion of the conductive layer. However, Juskey discloses forming a solder resist layer over the substrate 160, so as to define a void portion over the void portion. Thus, the solder resist when attached to the laminate of Hegel would be over the conductive layer, so as to define a void portion over the void portion of the conductive layer. Furthermore, it is well known the semiconductor industry to have a substrate having at least one resin layer as evident by Juskey (see col. 3 lines 20-25). Therefore, it would have been obvious to incorporate the solder resist with the process of Hegel, since the solder resist would facilitate the formation of metal patterns on the laminate that are used as connection areas for bonding wires extending from the chip as taught by Juskey.

With respect to Claims 33, 41, and 42, Hegel discloses wherein the underlying cavity 21, the void 21 portion of the third laminate layer, the void 21 portion of the fourth laminate layer, the void portion 21 of the conductive layer taught by Hegel and the void portion 150 of the solder resist layer taught by Juskey are formed to collectively form a void (see Figs. 2 of Juskey and Fig. 4 of Hegel).

With respect to Claim 34, Juskey discloses placing a die 130 over at least a portion of the solder resist layer 180 and forming an encapsulant 110 over the solder resist layer 180, over the die 130, and in the void 150 (see Fig. 2).

With respect to Claim 43, Hegel discloses wherein the encapsulant 16 is formed in substantially the entire void 21 (see Fig. 4).

With respect to Claim 44, Juskey discloses wherein the at least one resin layer is formed from bismaleimide triazine laminate (see col. 3 lines 20-25).

With respect to Claim 50, Juskey discloses wherein the void 150 having a varying profile since the voids are not plated with metal (see col. 3 lines 43-55; Fig. 2).

With respect to Claim 52, Juskey disclose a void 150 with a varying profiled (see Fig. 2). The changing shape of the structure is an obvious matter of design choice within ordinary skill in the art and a difference in the shape of the structure does not make the device operating differently. Note, the instant specification does not describe T-shaped profile as essential or critical or the only shape that could operate the claimed invention. In re Peters , 723 F.2d 891, 221 USPQ 952 (Fed. Cir. 1983). Therefore, it would have been obvious to incorporate a varying T-shaped profile as the void with Juskey, since the T-shaped profile would improve the attachment of the flow formed cover to the substrate as the varying void taught by Juskey.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hegel (U.S. 5,255,157) and Juskey et al. (U.S. 5,336,931) as applied to claims 33 and 40 above, and further in view of Papathomas (U.S. 5,623,006) and Marrs et al. (U.S. 5,355,283).

With respect to Claim 45, Hegel-Juskey both fail to disclose wherein the at least one resin layer is formed from FR-4 epoxy-glass laminate. However, Papathomas discloses wherein the at least one resin layer is formed from FR-4 epoxy-glass laminate (see col. 8 lines 35-45). Therefore, it would have been obvious to substitute the FR-4 epoxy glass for the material of the laminate taught by Hegel-Juskey, since substrates made of FR-4 epoxy glass perform well at high temperatures as taught by Papathomas.

With respect to Claim 51, it is well known in the semiconductor industry to have a void having a varying profile that is formed by a process drilling as evident by Marrs (see col. 5 lines 3-8).

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 30, 32-34, 40-45, and 50-52 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,423,581. Although the conflicting claims are not identical, they are

not patentably distinct from each other because claim 4 recites a laminate having first and second surfaces with at least a void while the instant application claims a laminate with first and second major faces with at least one void in the laminate extending from one of the major faces.

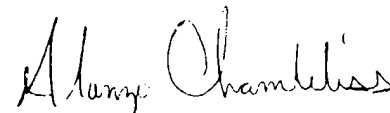
The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

12. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

AC/May 8, 2003



Alonzo Chambliss
Patent Examiner
Art Unit 2827